UNITED STATES PATENT AND TRADEMARK OFFICE

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>19 May 2008</u>.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-23</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-23</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

        1.☐ Certified copies of the priority documents have been received.

        2.☐ Certified copies of the priority documents have been received in Application No. _____.

        3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

1.   This office action is in response to communication filed on 5/19/2008

2.   The final rejection mailed on 2/20/2008 has been withdrawn.

3.   Claims 1-23 remain pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4.   Claims 1-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hollander

(USPN 6,182,258) in view of Thompson et al. (USPGN 2004/0093476).

As per claim 1,

Hollander discloses

A method stored on a computer readable medium including computer executable

instructions for automatically generating at least one test for testing a simulation model

of a device under test (DUT) in a test environment during a test verification process(see

Fig. 1), the method comprising:

providing a plurality of scenarios(c12: 3-10, "...the verification tests are

generated...)

automatically generating the test from said at least one selected scenario to provide at

least one input for driving simulated operation of the DUT `(c2: 24-32, "... a`

`program that drives…tests vectors into the DUT simulator…")`.

Hollander does not specifically disclose

each scenario featuring at least: one constraint relating to a relationship with at least one

other scenario; selecting at least one of said plurality of scenarios according to said

at least one constraint by resolving conflicts among said constraints of said

plurality of scenarios;

However, Thompson discloses

each scenario featuring at least: one constraint relating to a relationship with at least one

other scenario; selecting at least one of said plurality of scenarios according to said

at least one constraint by resolving conflicts among said constraints of said

plurality of scenarios; `([0001], "…preventing memory usage conflicts`

`when generating and merging test cases…",[0003], "...memory`

`segment used is noted...")`

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the

invention was made to incorporate the teachings of Thompson into the teachings of Hollander

to include the limitation discloses by Thompson. The modification would be obvious to one of

ordinary skill in the art to want to have desired behavior of test scenarios as suggested by

Thompson ([0002], "…otherwise the desired behavior of individual test cases will not occur.").

As per claim 2,   the rejection of claim 1 is incorporated;

Thompson discloses

selecting a number of said plurality of scenarios according to meta-data contained in at

least one scenario; and combining said number of said plurality of scenarios to form a

combined scenario instance ([0001], "…preventing memory usage conflicts

when generating and merging test cases…",[0003], "...memory

segment used is noted...").

As per claim 3,   the rejection of claim 2 is incorporated;

Hollander discloses

wherein at least one selected scenario comprises a sequence (c20, 15-20,

"…sequence is also…generated…").

As per claim 4,   the rejection of claim 3 is incorporated;

Thompson discloses

at least one selected scenario conflicts with at least one non-selected scenario and

wherein said meta- data comprises information about said conflict ([0003], "…not

overlapping…test cases, is assigned…" those that are not assigned

are non-selected.")

As per claim 5,   the rejection of claim 1 is incorporated;

Hollander discloses

said selecting at least one of said plurality of scenarios is performed at least partially

according to a configuration of the DUT`(c2:50-57, "Parameter driven test`

`generation…")`.

As per claim 6,   the rejection of claim 1 is incorporated;

Thompson discloses

said providing said scenarios is performed during a scenario creation process`([0029],`

`"…test case for a target processor…")`.

As per claim 7,

the rejection of claim 6 is incorporated;

Hollander discloses

a user performs said scenario creation process`(c5: 8-12, "…The user has full`

`control of…generation process.")`.

As per claim 8,   the rejection of claim 1 is incorporated;

Hollander discloses

said providing said plurality of scenarios is performed by a user`(c5: 8-12, "…The`

`user has full control of…generation process.")`.

As per claim 9,   the rejection of claim 1 is incorporated;

Hollander discloses

Generating at least one external file according to said at least one scenario (c9: 1-5,

"…test files…").

As per claim 10,   the rejection of claim 9 is incorporated;

Hollander discloses

Using said at least one external file at run time for running the test(c9: 1-5, "…test

files…is used to run tests").

As per claim 11,   The method of claim 10 further comprising:

Hollander discloses

compiling said at least one external file before said using said at least one external

file(c14: 58-62, "…or compiled…").

As per claim 12,   the rejection of claim 10 is incorporated;

Hollander discloses

wherein said generating said at least one external file is performed before or

concurrently with said generating said test(c9:3-7, "…test file is uses to

run tests." Therefore it at least concurrently.).

As per claim 13, the rejection of claim 10 is incorporated;

Hollander discloses

wherein said external file comprises an HDL (hardware description language) file for

configuring the simulation model `(c5: 52-56, "...support...HLVA...")`.

As per claim 14, the rejection of claim 1 is incorporated;

Hollander discloses

said generating the test is performed according to an at least partially randomized

process `(c5: 8-11, "...random generation process...")`.

As per claim 15, the rejection of claim 14,

Thompson discloses

said randomized process is based upon a plurality of constraints, and wherein said

plurality of constraints is provided in said selected scenario `([0039], "...randomly to`

`determine...")`.

As per claim 16, the rejection of claim 1 is incorporated;

Thompson discloses

> wherein said generating the test is performed according to said at least one
>
> constraint([0002]).

As per claim 17,   the rejection of claim 16 is incorporated;

Thompson discloses

> each constraint defines a type of expected input variable and a type of operation to be
>
> performed, on said type of expected input variable([0003], "…segment of memory
>
> which it can use…").

As per claim 18,   the rejection of claim 17 is incorporated;

Thompson discloses

> said constraint comprises a static constraint on a value of said type of expected input
>
> variable([0003], "…segment of memory which it can use…").

As per claim 19,   the rejection of claim 17 is incorporated;

Thompson discloses

> said constraint comprises a dynamic constraint on a value of said type of expected input
>
> variable([0029], "…memory range for each case…").

As per claim 20,   the rejection of claim 17 is incorporated;

Hollander discloses

>   said at least one type of expected input variable is at least partially determined according
>
>   to a simulation model of the DUT `(c2:50-57, "Parameter driven test`
>
>   `generation…")`.

.

As per claim 21,   the rejection of claim 1 is incorporated;

Thompson discloses

>   at least one characteristic of said constraint determines whether said constraint conflicts
>
>   with another constraint`([0029], "…memory range for each case…")`.

As per claim 22,   the rejection of claim 1 is incorporated;

Hollander discloses

>   the simulation model comprises a plurality of variables`(c10: 3-8, Verilog`
>
>   `variables…")`,   wherein at least one scenario comprises a monitoring operation for
>
>   monitoring behavior of the simulation model and wherein said monitoring operation
>
>   comprises sampling at least one value of at least one variable of the simulation
>
>   model(c3: 29-34, "…sample the device model…").

Claim 23.   the rejection of claim 1 is incorporated;

Thompson discloses

> The selecting at least one of said plurality of scenarios according to said at least one
>
> constraint is accomplished by automatically selecting a subset of said plurality of
>
> scenarios by resolving said constraints of said plurality of scenarios to include in
>
> the selected subset only non-conflicting scenarios (`[0003]`, "…not
>
> `overlapping…test cases, is assigned…`" those that are not assigned
>
> are non-selected.")

Response to Arguments

5.   Applicant's arguments have been considered but are moot in view of the new ground(s)

of rejection.

Conclusion

THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the

extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Philip Wang whose telephone number is 571-272-5934. The examiner can normally be reached on Mon - Fri 8:00 - 4:00PM. Any inquiry of general nature or relating to the status of this application should be directed to the TC2100 Group receptionist: 571-272-2100.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wei Zhen can be reached on 571-272-3708. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Wei Y Zhen/

Supervisory Patent Examiner, Art Unit 2191